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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MALDONADO, JULIO J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,207	MIURA ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-36* is/are pending in the application.

4a) Of the above claim(s) *34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-33,35 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 23-27 is withdrawn in view of the newly discovered reference(s) to Bryant et al. (U.S. 5,376,571) and Wolf et al. (Silicon Processing for the VLSI Era, Volume: Process Technology). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15-32 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo (U.S. 5,668,403) in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1: Process Technology).

In reference to claim 15, 18, 21-24, 26, 28-32 and 35, Kunikiyo (Figs.1-10) teaches a method of forming element separating oxides during the manufacture of MOSFET devices including the steps of oxidizing a main surface of a silicon substrate (1); forming an oxidation-preventing film (3) made of silicon nitride on portions of the oxidized (2) silicon substrate (1); removing part of the oxidation-preventing (3) film that is located in an element-separating area (4); forming the element separating oxide (7) film on the silicon substrate (1) in the element-separating area (4) after removing the part of the oxidation-preventing film (3); removing the rest of the oxidation-preventing

film (3); performing a heat treatment at a temperature of 800°C or higher in an inert atmosphere in a bare state; implanting impurity ions (6) on the substrate; and forming a MOSFET (8) on the surface of the substrate including forming a gate oxide, a gate electrode and self aligned source and drain regions (Fig.7) (column 8, line 11 – column 9, line 44).

Kunikiyo fails to teach forming thermal oxide films on the silicon substrate by oxidizing the silicon substrate; and after forming thermal oxide in an element-forming area, carrying out a heat-treatment at a temperature of 800°C or higher in an inert atmosphere. However, Wolf et al. teach that is common practice within the art in of forming implanted regions to form a thin layer of silicon dioxide by thermal oxidation prior to ion implantation to screen against metals or other contaminants during the implantation process (Wolf et al., pages 198-199 and page 323), and annealing after an implantation process in an inert atmosphere at temperatures of 900-100°C to correct crystalline damage cased by the implantation process (Wolf et al., page 305). Furthermore, Wolf et al. teach that thermal oxides are formed in water containing atmospheres and wherein other applications to the thermal oxide formation process includes gate oxides and isolation of individual devices, e.g. local oxidation of silicon (LOCOS), wherein using thermal oxide processes provide the further advantage of provide an oxide layer with thickness control (Wolf et al., page 198). Still further, Wolf et al. teach using ion implantation to form self-aligned source/drain regions in a MOS device (Wolf et al., page 322).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kunikiyo and Wolf et al. to enable forming the thermal oxides and also the heat treatment processes as taught by Wolf in the process of Kunikiyo.

In reference to claims 16 and 19, the combination of Kunikiyo and Wolf et al. teach wherein the heat treatment is carried out in an atmosphere of an inert gas selected from nitrogen, said gas mixture being able to contain 5% or less of oxygen (Kunikiyo, column 8, lines 24 – 27, and column 10, lines 53 – 64 and Wolf et al., page 305).

In reference to claims 17, 20, 22, 25 and 27, the combined teachings of Kunikiyo and Wolf et al. teach wherein the oxide film is kept in a bare state during the heat-treatment for stress relaxation (Kunikiyo, column 8, lines 20 – 49). The combination of Kunikiyo and Wolf et al. fail to expressly teach wherein the heat-treatment is carried out for relaxation of stress in the gate electrode film. However, the same materials would be treated the same way and therefore the same results would be obtained. Therefore the prior art of record teach upon the claimed limitation.

4. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunikiyo (U.S. 5,668,403) in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1: Process Technology) as applied to claims 15-32 and 35 above, and further in view of Chen et al. (U.S. 5,413,950).

The combined teachings of Kunikiyo and Wolf et al. fail to further teach wherein the semiconductor device is a DRAM device. However, Chen et al. teach a method of

forming element-separating oxides and MOSFET devices as part of the formation of DRAM devices (column 4, lines 24 – 33). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further use the teachings of Kunikiyo and Wolf et al. to form a DRAM device as evidenced by Chen et al.

5. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bryant et al. (U.S. 5,376,571) in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1: Process Technology).

Bryant et al. (Figs.3-5) teach a method of forming a semiconductor device including the steps of forming an element separating oxide (not shown) on the surface of a substrate (20); forming a tunnel oxide film (22) on the semiconductor substrate (20); forming a floating electrode (24) on the tunnel oxide film (22); forming an insulating film (26) on the floating electrode (24); forming a controlling electrode (28) on the insulating film (26); and self-aligned forming implanted regions (36, 42) on the surface of the substrate (20) after forming said controlling electrode (28) (column 4, line 29 – column 5, line 20).

Bryant et al. fail to teach subjecting the semiconductor substrate on which the controlling electrode is formed to a heat-treatment at a temperature of 800°C. However, Wolf et al. teach that is common practice within the art of forming implanted regions to anneal a substrate after an implantation process in an inert atmosphere at temperatures of 900-100°C to correct crystalline damage cased by the implantation process (Wolf et al., page 305).

Therefore, it would have been obvious tone of ordinary skill in the art at the time the invention was made to perform the heating process after the implantation step as taught by Wolf et al.

Response to Arguments

6. Applicant's arguments with respect to claims 15-33, 35 and 36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
January 20, 2005

George Fourson
Primary Examiner